AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (currently amended) A variable width memory system comprising:

a bus for communicating information;

a plurality of single cell variable width memory locations coupled to said bus, said plurality of single cell variable width memory locations store information, wherein said plurality of single cell variable width memory locations receive a number of bits corresponding to the width of the single cell variable width memory locations and the width of a variable width register; and

a controller coupled to said bus, said controller directs access to said plurality of single cell variable width memory locations, wherein said number of bits potentially vary automatically on a per access basis depending on which single cell variable width memory location of said plurality of single cell variable width memory locations is being accessed, wherein all memory locations are not required to have the same width.

2. (previously presented) The variable width memory system of Claim 1 wherein said plurality of single cell variable width memory locations are included on a single memory substrate.

3. (previously presented) The variable width memory system of Claim 1, wherein said plurality of single cell variable width memory locations are included in a random access memory (RAM).

4. (previously presented) The variable width memory system of Claim 1, wherein each one of said plurality of single cell variable width memory locations is identified by a unique

internal identifier which is referenced by said controller to access said each one of said plurality of single cell variable width memory locations.

5. (original) The variable width memory system of Claim 4, wherein said controller maps said unique internal identifier to a particular external indicator, wherein components referred to by said unique internal identifier and said particular external indicator have the same bit width.

6. (previously presented) The variable width memory system of Claim 1, wherein the bit width of at least two of said plurality of single cell variable width memory locations is the same.

7. (previously presented) The variable width memory system of Claim 1, wherein the bit width of at least one of said plurality of single cell variable width memory locations is configured in accordance with criteria directed at decreasing processor operations.

8. (previously presented) A variable width memory mapping method comprising:

receiving a register indicator corresponding to a register;

accessing a single memory cell based on said register indicator, wherein said single memory cell is allocated a storage size correlating to the bit capacity of said register;

transferring information between said single memory cell and another component, wherein said information includes the same number of bits as said bit capacity; and

potentially varying the bit capacity of said register on a per access basis to memory cells automatically, wherein all memory locations are not required to have the same width.

9. (original) The variable width memory mapping method of Claim 8 wherein said register indicator is received from a processor.

10. (original) The variable width memory mapping method of Claim 8 wherein said bit capacity is determined by processing criteria associated with a processor.

11. (original) The variable width memory mapping method of Claim 8 wherein said information is part of a communication packet.

12. (original) The variable width memory mapping method of Claim 8 wherein said information includes data associated with certain fields.

13. (original) The variable width memory mapping method of Claim 12 wherein bits included in said data associated with certain fields are sequentially located within said memory cell.

14. (original) The variable width memory mapping method of Claim 8 wherein a information storage system with a computer readable medium stores information in accordance with said variable width memory mapping process.

15. (canceled)

16. (previously presented) The variable memory width assignment method of Claim 20 wherein said memory location is one of a plurality of memory locations of various widths.

17. (previously presented) The variable memory width assignment method of Claim 20 wherein said memory location has a unique identifying address.

18. (previously presented) The variable memory width assignment method of Claim 20 further comprises providing an association between said memory location and an external identifier.

19. (previously presented) The variable memory width assignment method of Claim 20 wherein said bits in said portion of said data block are arranged in a contiguous manner.

20. (currently amended) A variable memory width assignment method comprising:

analyzing a ~~data block~~ register configuration specification;

identifying bits in a portion of said ~~block of data~~ register, wherein said portion corresponds to information grouped in an arrangement that facilitates reduction of processing instructions;

assigning a memory location a width equal to the number of said bits in said portion of said ~~block of data~~ register, wherein said ~~data block~~ register is arranged in accordance with a communications packet configuration specification; and wherein the number of said bits potentially vary automatically on a per access basis to portions of said ~~blocks of data~~ register when identifying said bits and said width potentially vary automatically on a per access basis when assigning a single cell memory location that is equal to the number of said bits, wherein all memory locations are not required to have the same width.

21. (canceled)

22. (canceled)

23. (currently amended) A variable width memory assignment system comprising:

a means for communicating memory location identifiers;

a means for storing information in uniquely identifiable different width single cell memory locations corresponding to said memory location identifiers, wherein said means for storing said information returns the number of bits equal to the width of one of said uniquely identifiable different width single cell memory locations and the width of a register in response to a read request, wherein the number of bits returned by said means for storing information are potentially varied automatically per read request due to which of said

uniquely identifiable different width single cell memory locations is being accessed by said read request; and

a means for managing a connection with said uniquely identifiable different width single cell memory locations, wherein said means for managing said connection supervises writing and reading of information to and from said uniquely identifiable different width single cell memory locations, wherein all memory locations are not required to have the same width.

24. (previously presented) The variable width memory assignment system of Claim 23 wherein said means for managing said connection includes a means for tracking a correspondence between said uniquely identifiable variable memory widths and register identifiers.

25. (original) The variable width memory assignment system of Claim 24 wherein said register identifiers are provided by a means for processing said information.